REMARKS

Claims 1-25 remain pending in the current Application. Claims 1, 3, 10, 13-15, and 18 have been amended; and claims 23-25 have been added. No other amendments to the claims have been made herein. Applicants submit that the amendments do not add new matter to the current Application. All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicants also submit that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Claim Rejections under 35 U.S.C. 102 and 103(a)

Claims 1 – 2 and 21

Applicants respectfully submit that claims 1 - 2 and 21 are patentable under 35 U.S.C. 103(a) over Hennessy in view of US Patent No. 4,541,045 (hereinafter referred to as Hennessy). Applicants have amended claim 1 to further clarify the current address with respect to the previous address. Claim 1, as amended, claims "wherein the current address follows the previous address without any intervening addresses." Therefore, each of the first and second signals is negated with respect to these addresses, and the third signal is negated with respect to a current address, if it is an instruction address, and an immediately preceding instruction address. (Note that Applicants have also amended claim 1 to further clarify the third sequence signal.) In the response to the Arguments section in the Final Rejection, the Examiner clarified for the Applicants that the Examiner defined the current address "as the correct address at which instructions must be fetched from after the branch instruction." That is, the Examiner refers to the branch target address as the current address. Therefore, if the Examiner defines the current address as the correct address at which instructions must be fetched from after the branch instruction (i.e. the branch target address), then the previous instruction refers to the address previous the current address without any intervening addresses. With this clarification of the current and previous addresses in claim 1, Applicants submit that Hennessy, Kromer, nor their

combination teach or suggest all the elements of claim 1. The Examiner states that Hennessy's branch prediction scheme teaches the first and second sequence signals. For example, the Examiner states that the branch prediction is the first sequence signal in that, when negated, it indicates if a current address (the branch target address) may not be sequential to a previous address (the branch instruction address) and states that the second sequence signal is the one which represents the actual outcome of the branch. However, the previous address in claim 1 refers to a previous address without any intervening addresses. Therefore, the branch prediction signal of Hennessy, does not indicate whether the branch target address, when finally resolved, is not sequential to the address that is immediately previous to that branch target address. At most, it indicates whether the address representing the correct outcome of the branch may not be sequential to the branch instruction itself, since it is only a prediction. Furthermore, the signal representing the actual outcome of the branch does not indicate whether this address is not sequential to an immediately previous address, instead it simply indicates whether the branch prediction was correct or not, providing no information as to the sequentialness of the branch target address to an immediately preceding address. Therefore, neither the branch prediction signal nor the signal representing the actual outcome of the branch provides any information regarding the sequentialness of the actual outcome of the branch (the correct address at which instruction may be fetched from after the branch instruction) and an immediately previous address.

Still referring to claim 1, the Examiner states that the VALID + .5 signal of Kromer teaches the third sequence signal of claim 1 that when asserted indicates that the current address, if it is an instruction address, is sequential to an immediately preceding instruction address, and when negated, indicates that the current address, if it is an instruction address, is not sequential to the immediately preceding instruction address. In the Response to Arguments section, the Examiner clarified that he assumed the current address to be the correct address at which instructions must be fetched from. Therefore, in rejecting claim 1 over Kromer, the Examiner points to 80 (i.e. IN) of Figs. 2A and 2C as the current address, with the VALID+.5 signal being the third sequence signal. However, when VALID+.5 is negated, it only indicates that a current instruction (the target of a jump instruction, e.g. 80 or IN) may not be sequential to the jump instruction (at I3/I4), but does not indicate that the current instruction (80 or IN) is not sequential to I5, the immediately preceding instruction address. Furthermore, when VALID+.5 is asserted, it does not indicate that the current address (i.e. 80 or IN) is sequential to I5. That is, VALID+.5 does not indicate any type of relationship between IN and I5. Therefore, for at least these

reasons, Applicants submit that Kromer does not teach or suggest a third sequence signal as claimed in claim 1.

Therefore, for at least these reasons, Applicants submit that claim 1 is allowable over Hennessy in view of Kromer. Claims 2 and 23 have not been independently addressed because they depend directly or indirectly from allowable claim 1 and are therefore also allowable for at least those reasons provided above with respect to claim 1.

Claims 3 - 9

Applicants respectfully submit that claims 3-9 are patentable over Hennessy in view of Kromer. With respect to claim 3, Applicants have also clarified current address by including "wherein the current address refers follows the previous address without any intervening addresses," and have also further clarified the third sequence signal Therefore, as discussed above with respect to claim 1, Hennessy, Kromer, nor their combination teach, or suggest first and second sequence signals provided for a current address and a previous address, as claimed in claims 1 and 3. Many of the same arguments provided above with respect to claim 1 apply to claim 3; therefore, claim 3 is allowable over the cited references for at least those reasons provided above with respect to claim1.

Claims 4-9 have not been independently addressed because they depend directly or indirectly from allowable claim 3 and are therefore also allowable for at least those reasons provided above with respect to claim 3.

Claims 10-12

Applicants respectfully submit that claims 10-12 are patentable under 35 U.S.C. 102 over Kromer. With respect to claim 10, Applicants submit that Kromer does not teach or suggest each and every element of claim 10. For example, claim 10 claims an address bus for providing a current address (for retrieving a first instruction), a previous address (for retrieving a second instruction), and a data address wherein the data address occurs before the current address and after the previous address. Furthermore, claim 10 claims a fetch unit for generating a first sequence signal that when asserted indicates that the current address is sequential to the previous address and when negated indicates that the current address may not be sequential to the previous address. Applicants have also amended claim 10 to further clarify the current address

by claiming "wherein the current address follows the previous address without any intervening addresses for retrieving instructions." Kromer does not teach or suggest these elements.

With respect to claim 10, the Examiner states that the VALID + .5 signal of Kromer teaches a first sequence signal that when asserted indicates that the current address is sequential to the previous address, and when negated, indicates that the current address may not be sequential to the previous address. In the Response to Arguments section, the Examiner clarified that he assumed the current address to be the correct address at which instructions must be fetched from. Therefore, in rejecting claim 10 over Kromer, the Examiner points to 80 (i.e. IN) of Figs. 2A and 2C as the current address, with the VALID+.5 signal being the first sequence signal. However, Applicants have further clarified the previous address as the immediately preceding instruction address. Therefore, if the Examiner assumes the VALID+.5 to be the first sequence signal, then when VALID+.5 is negated, it only indicates that a current instruction (the target of a jump instruction, e.g. 80 or IN) may not be sequential to the jump instruction (at I3/I4), but does not indicate that the current instruction (80 or IN) may not be sequential to I5, the immediately preceding instruction address. Furthermore, when VALID+.5 is asserted, it does not indicate that the current address (i.e. 80 or IN) is sequential to I5. That is, VALID+.5 does not indicate any type of relationship between IN and I5. Therefore, for at least these reasons, Applicants submit that Kromer does not teach or suggest a first sequence signal as claimed in claim 10.

Claims 11-12 have not been independently addressed because they depend directly or indirectly from allowable claim 10 and are therefore also allowable for at least those reasons provided above with respect to claim 10.

Claims 13-17 and 22

Applicants respectfully submit that claims 13-17 and 22 are patentable under 35 U.S.C. 103 over Samra in view of Oh and under 35 U.S.C. over Hennessy. Applicants have amended claim 13 to clarify operation of the first and second sequence signals. Applicants submit that Samra, Oh, and Hennessy, alone or in combination, do not teach or suggest each and every element of claim 13, as amended. For example, claim 13 claims a fetch unit for providing a first sequence signal and a second sequence signal for each address provided on the address bus wherein the first sequence signal indicates whether each address provided on the address bus may be sequential to an immediately preceding address on the bus and a second sequence signal

that indicates whether each address provided on the bus is sequential to the immediately preceding address on the bus. None of the cited references, alone or in combination, teach, suggest, or provide motivation for a fetch unit which provides two signals for each address provided on the address bus as claimed in claim 13.

With respect to the rejection of claim 13 over Samra in view of Oh, the Examiner states that Oh's LATCH signal teaches the first sequence signal of claim 1 because it indicates that the current address (being some address generated during burst mode) may be sequential to the previous address because the burst mode may be set such that an access is occurring in sequential mode. However, Oh's LATCH signal is not provided for each address on an address bus to indicate whether each address on the bus may be sequential to an immediately preceding address on the bus. Oh's LATCH only denotes the beginning of a burst and thus is only asserted at the beginning of a burst cycle where subsequent counts of the burst are generated by the y-address counter. That is, for subsequent counts of the burst, the LATCH is ignored, providing no sequentialness information for each address during the burst. The Examiner also states seq_int#, when asserted, teaches the second sequence signal. However, these signals (the LATCH and seq_int#) are not both provided for each address on an address bus to provide sequentialness information as claimed in claim 13. Furthermore, there is no motivation in Oh to provide multiple signals for each address in the burst. Therefore, for at least these reasons, Applicants submit that claim 13 is allowable over Samra in view of Oh.

Applicants also submit that claim 13 is not taught or suggested by Hennessy. The Examiner states that Hennessy's branch prediction scheme teaches the first and second sequence signals. For example, the Examiner states that the branch prediction is the first sequence signal that the second sequence signal is the one which represents the actual outcome of the branch. However, neither of these signals provide sequentialness information for each address on an address bus with respect to an immediately preceding address on the bus, as claimed in claim 13. For example, the branch prediction address indicates that the actual outcome of the branch may or not be sequential to the branch instruction itself, since it is only a prediction. However, it does not indicate whether an address may be sequential to an immediately preceding address (as, for example, described above in reference to claim 1), and furthermore, does not indicate whether each address may be sequential to the immediately preceding address. Similarly, Hennessy's signal representing the actual outcome of the branch does not indicate whether each address on the bus is sequential to the immediately preceding address, it only indicates whether the previous

branch prediction was correct. Therefore, for at least these reasons, Applicants submit that claim 13 is allowable over Hennessy.

Therefore, for at least these reasons, Applicants submit that claim 13 is allowable over the cited references. Claims 14-17, 22, and 25 have not been independently addressed because they are allowable over the cited references for at least those reasons provided above with respect to claim 13.

Claims 18-20

Applicants respectfully submit that claims 18-20 are patentable over Kromer. With respect to claim 18, Applicants submit that Kromer does not teach each and every element of claim 18. Applicants have amended claim 18 to further clarify the first sequence signal. For example, claim 18 claims a fetch unit for providing a first sequence signal that indicates whether each instruction address provided on the address bus is sequential to an immediately preceding instruction address even if a data address is provided between the instruction address and the immediately preceding instruction address. Kromer does not teach or suggest these elements.

With respect to claim 18, the Examiner states that the VALID + .5 signal of Kromer teaches a first sequence signal. However, the VALID+.5 is not provided to indicate whether *each* instruction address is sequential to an immediately preceding instruction, as claimed in claim 18. It is only provides an indirect indication of sequentialness based on non-decodable instructions, such as I4. That is, VALID+.5 provides an indication for IN (the target address) with respect to I3. However, it does not provide sequentialness information, for example, for I5 with respect to I3 or IN with respect to I5, because while asserted, VALID+.5 only indicates that a non-decodable instruction has not been encountered (where, while VALID+.5 is asserted, instructions may or may not be sequential to immediately preceding instruction addresses.) For example, when VALID+.5 is negated for a non-decodable instruction such as the target address for a jump instruction (at, e.g., I4), it only indicates that the target of the jump instruction (IN) may not be sequential to the branch instruction (at I3), but does not indicate the sequentialness of the target instruction (IN) and the immediately preceding instruction address (I5). Similarly, when VALID+.5 is asserted in FIG. 2C, it does not indicate that each of the addresses are sequential to an immediately preceding instruction (e.g., note that IN is not sequential to I5). Therefore, for at least these reasons, Kromer does not teach or suggest a third sequence signal as claimed in claim 18.

Claims 19-20 have not been independently addressed because they depend directly or indirectly from allowable claim 18 and are therefore also allowable for at least those reasons provided above with respect to claim 18.

Added Claim 24

Applicants respectfully submit that claim 24 is allowable over the cited references. Claim 24 is similar to claim 3, prior to amendment herein, where Applicants have further clarified the first and second sequence signals. For example, claim 24 claims "wherein if the current address is not sequential to the previous address, the first sequence signal is negated prior to the second sequence signal being negated and the first and second sequence signals are negated in a same clock cycle." Applicants submit that Hennessy, Kromer, Samra, Oh, alone or in combination, do not teach or suggest this element of claim 24. Therefore, Applicants submit that claim 24 is also allowable.

Conclusion

Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action, yet reserve the right to address them at a later time if necessary.

Applicant respectfully solicits allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

Please charge any fees due to Deposit Account Number 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

By: _____

Joanna G. Chiu
Attorney of Record
Reg. No.: 43,629
Telephone:(512) 996-6839
Fax No.: (512) 996-6854

SEND CORRESPONDENCE TO:

Freescale Semiconductor, Inc.
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Customer Number 23125